Amendments to the specification:

Please replace paragraphs 1 and 2 on page 1 with the following revised paragraphs:

This application claims the benefits of provisional patent application Serial No. 60/262,401, filed January 16, 2001, for "Unilink Digital Architecture" (Docket No. RAL920010003US1).

This application is related to the following copending applications, all of which are incorporated herein by reference: Serial No. 09/996,091, filed November 28, 2001, for "Architecture For Advanced Serial Link Between Two Cards" (Docket No. RAL920010004US2); Serial No. 09/996,053, filed November 28, 2001, for "Analog Unidirectional Serial Link Architecture" (Docket No. RAL920010005US2); and Serial No. 09/997,587, filed November 28, 2001, for "Apparatus And Method For Oversampling With Evenly Spaced Samples" (Docket No. RAL920010011US2).

Please replace paragraph 2 on page 10 which continues as paragraph 1 on page 11 with the following revised paragraph:

The receiver analyzes the oversampled data stream and generates two sets of correlation output signals: the detected bit values and the early and late signals for an eventual update of the phase rotator. The early/late signals are generated by use of edge and data correlation tables of the type shown and described in copending patent application Serial No. 09/997,587, filed November 28, 2001, for "Apparatus And Method For Oversampling With Evenly Spaced Samples" (Docket No. RAL920010011US2). These tables provide a pattern recognition algorithm that serves to specify the early and late signals as a function of the input sample pattern. When the detected bit edge is centered between two samples, there is a 'dead-zone' in the clock and data recovery (CDR) control loop if no jitter is present. With a jitter number larger than the sample spacing, the loop will average the detected sample crossings and will position the edge in the middle between two samples. This is a different situation than that found in a PLL phase detector with a dead zone, because the jitter is much larger and the phase control is digital with no leakage effects. The probability of generating a metastable sampling output is reduced for a middle edge position because the probability of an edge being positioned right on a sample is reduced.